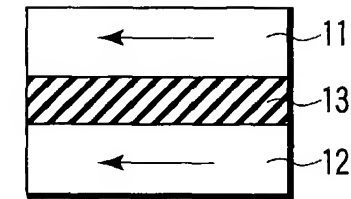
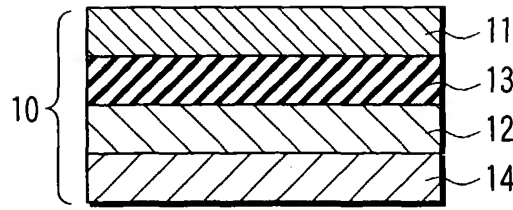
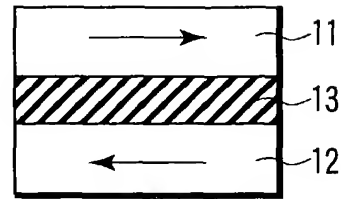


FIG. 1  
(PRIOR ART)



Parallel (Low resistance)

FIG. 2A  
(PRIOR ART)



Anti-parallel (High resistance)

FIG. 2B  
(PRIOR ART)

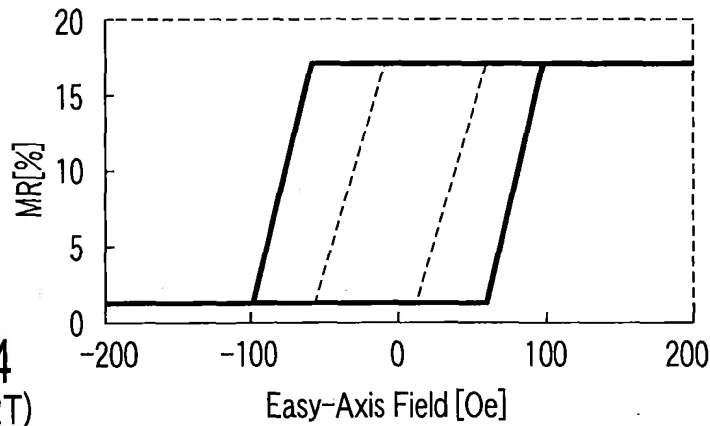


FIG. 4  
(PRIOR ART)

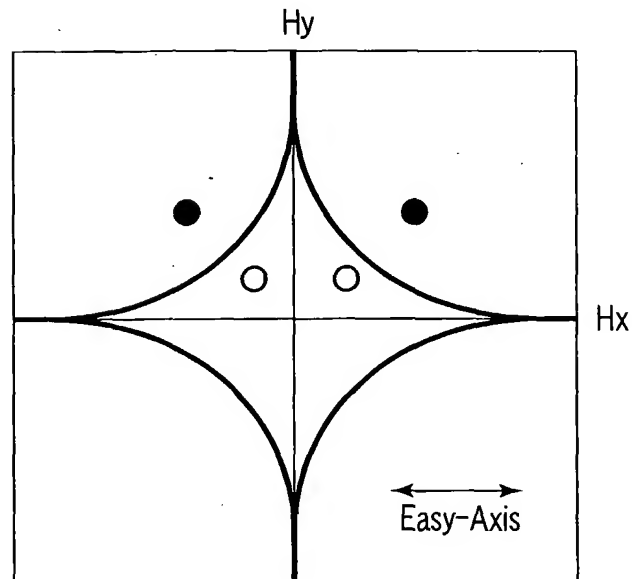


FIG. 5  
(PRIOR ART)

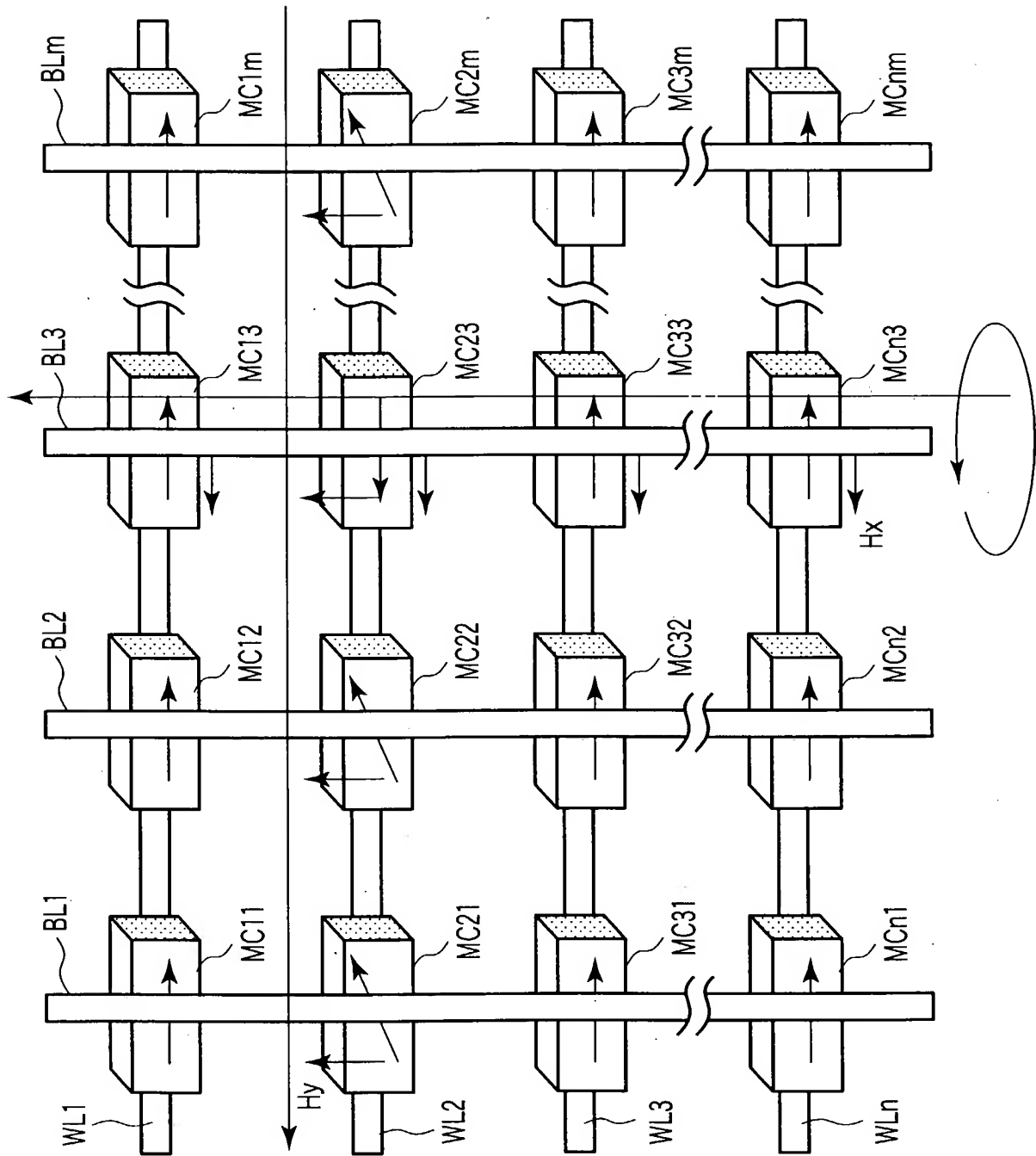


FIG. 3  
(PRIOR ART)

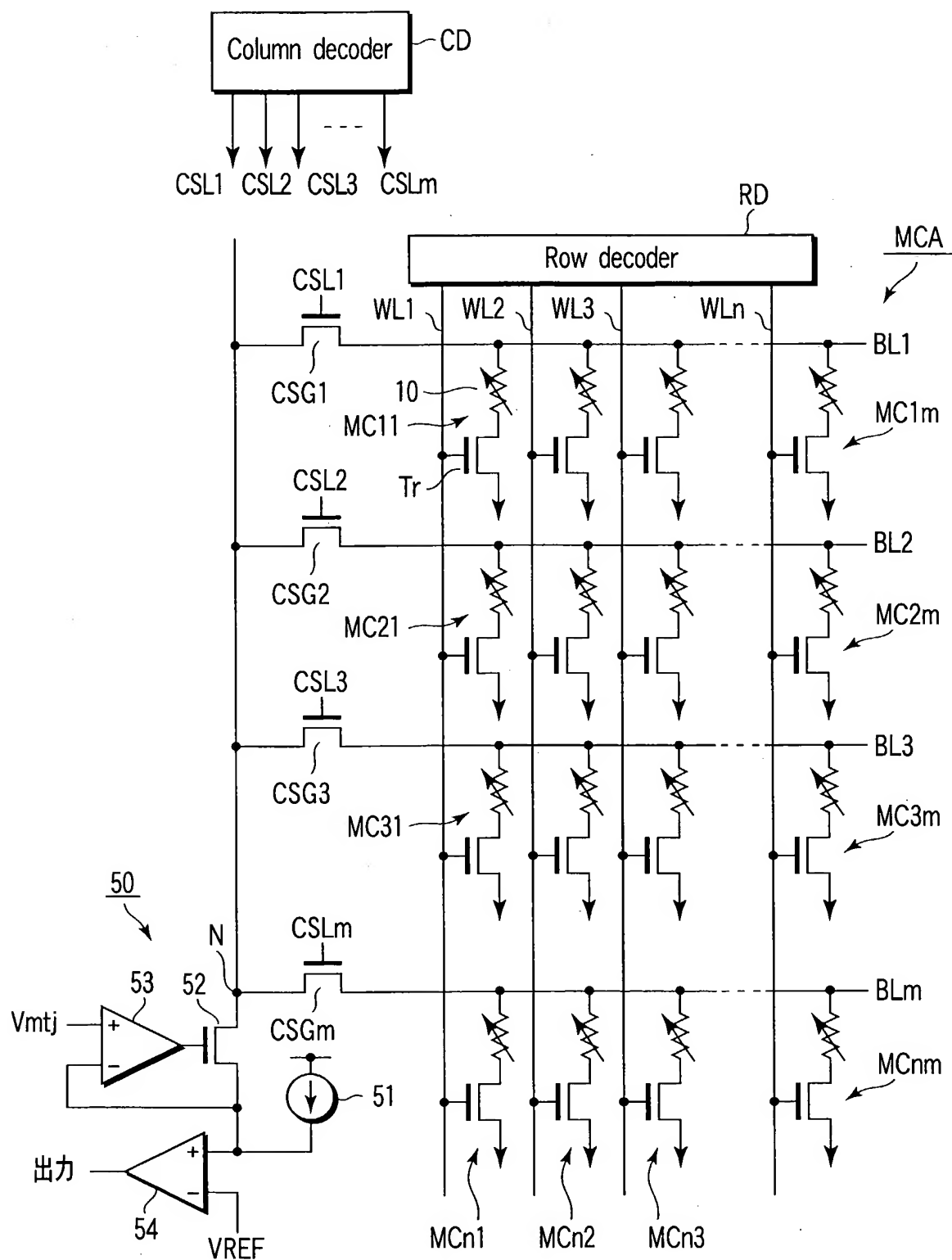


FIG. 6

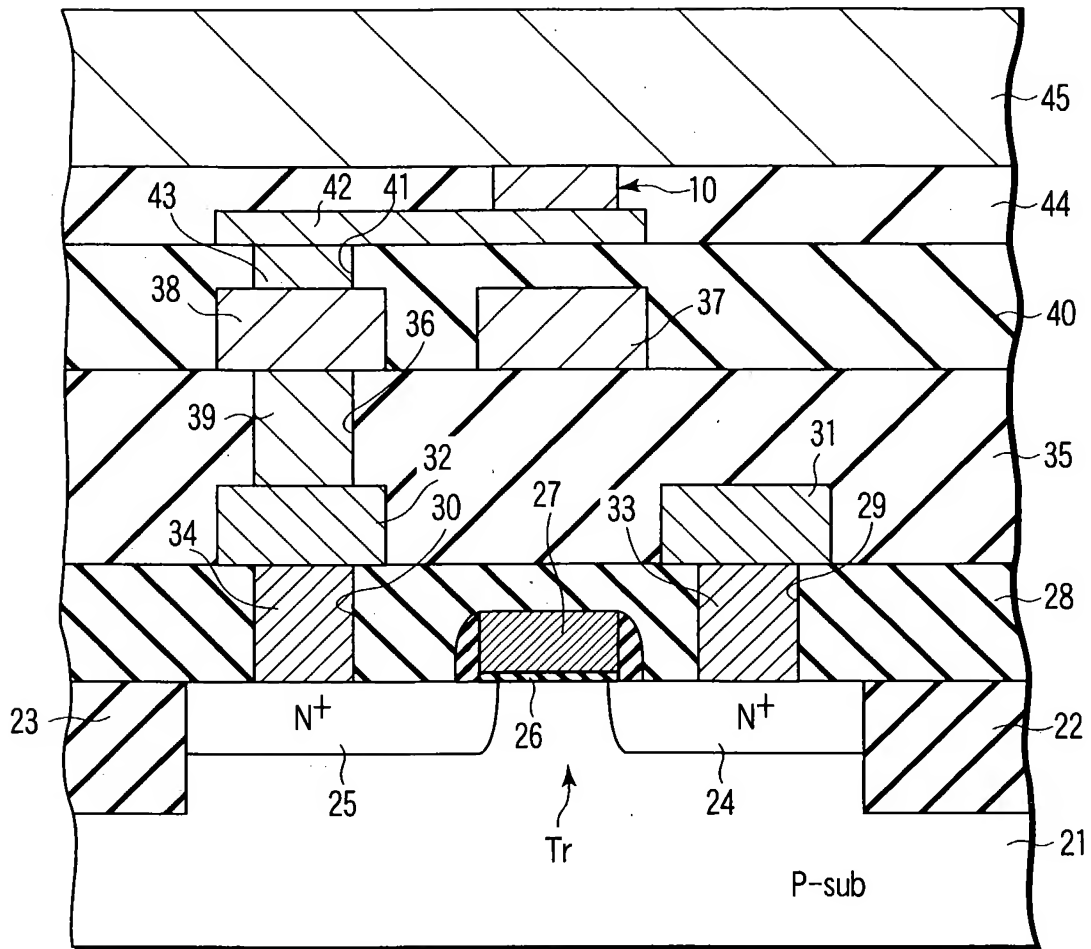


FIG. 7

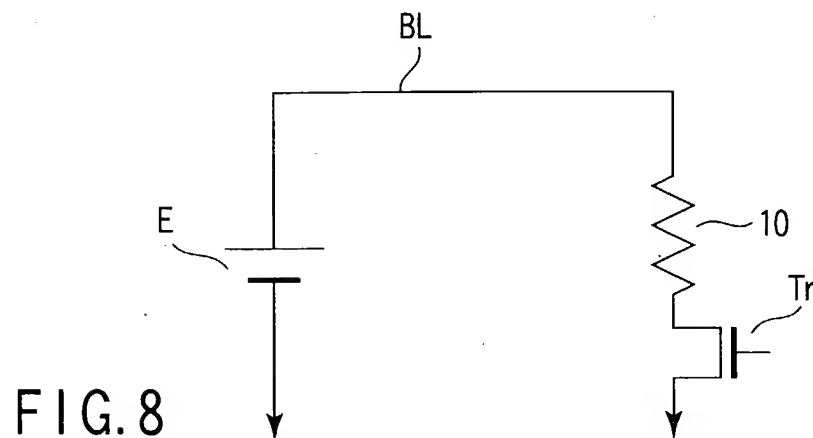


FIG. 8

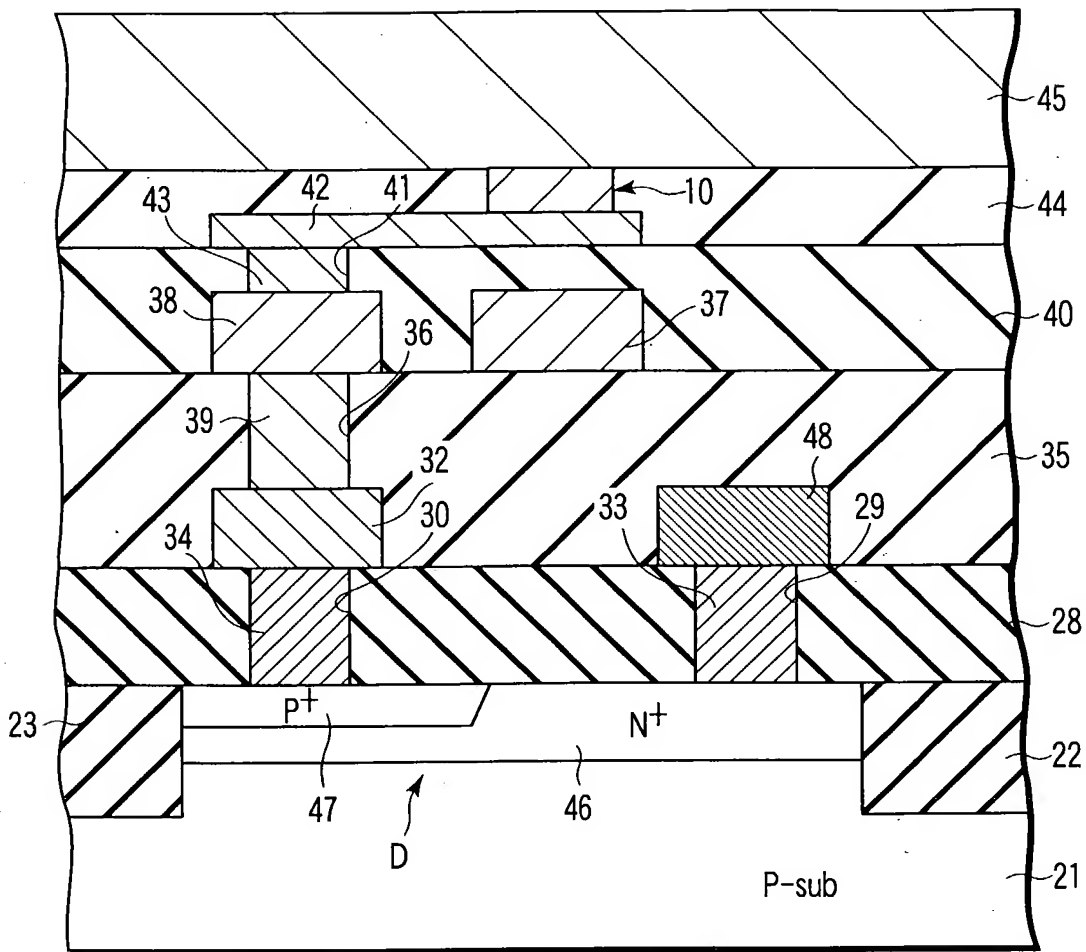
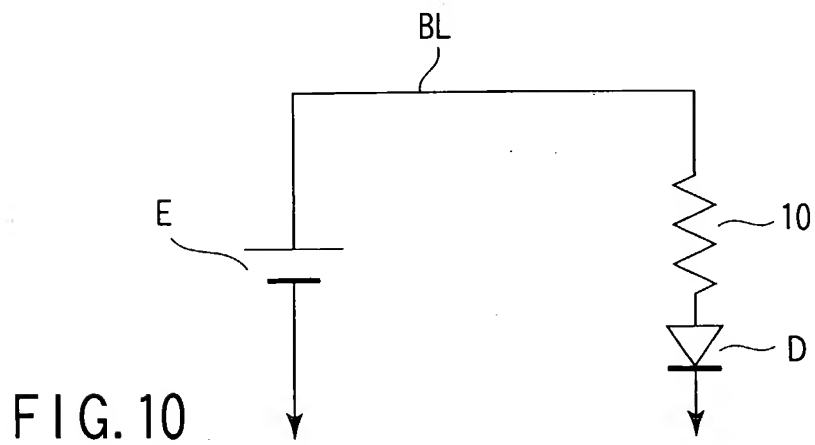


FIG. 9



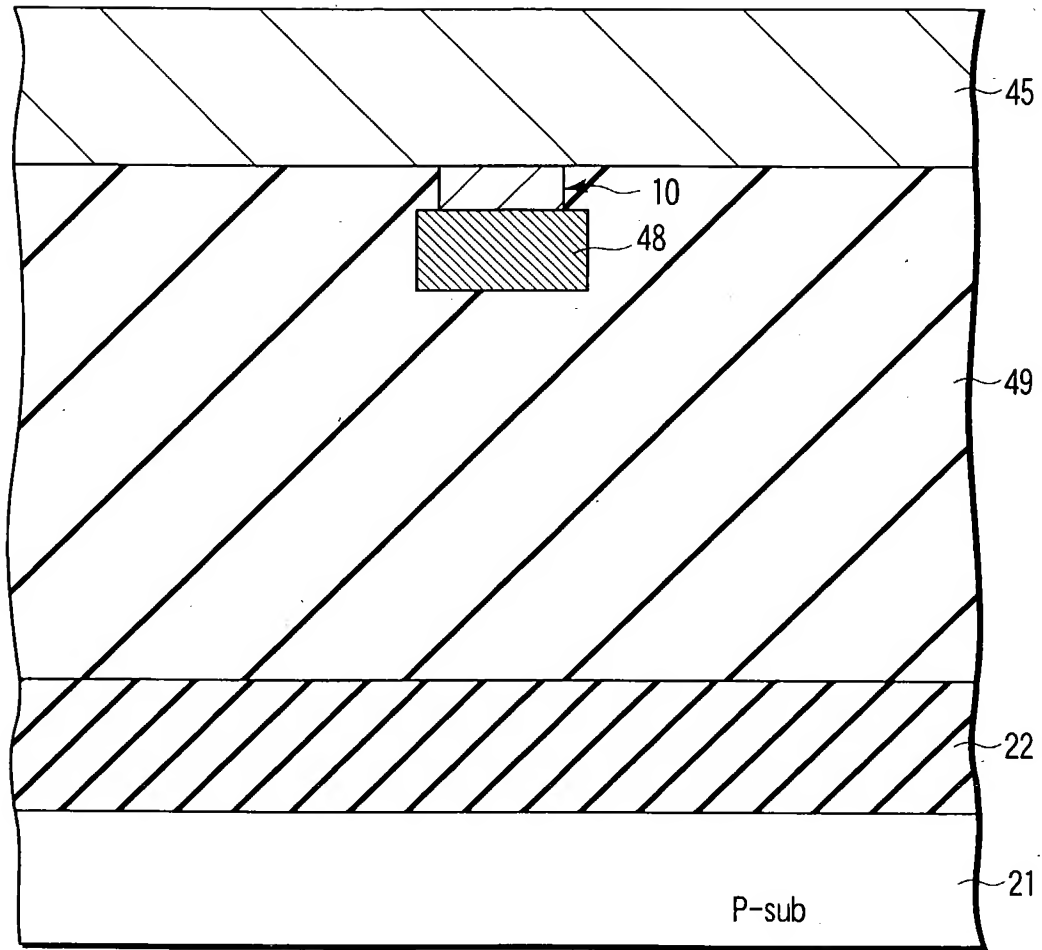


FIG. 11

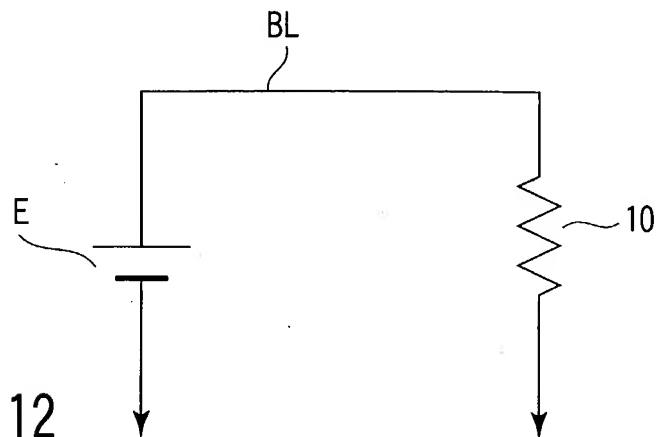


FIG. 12

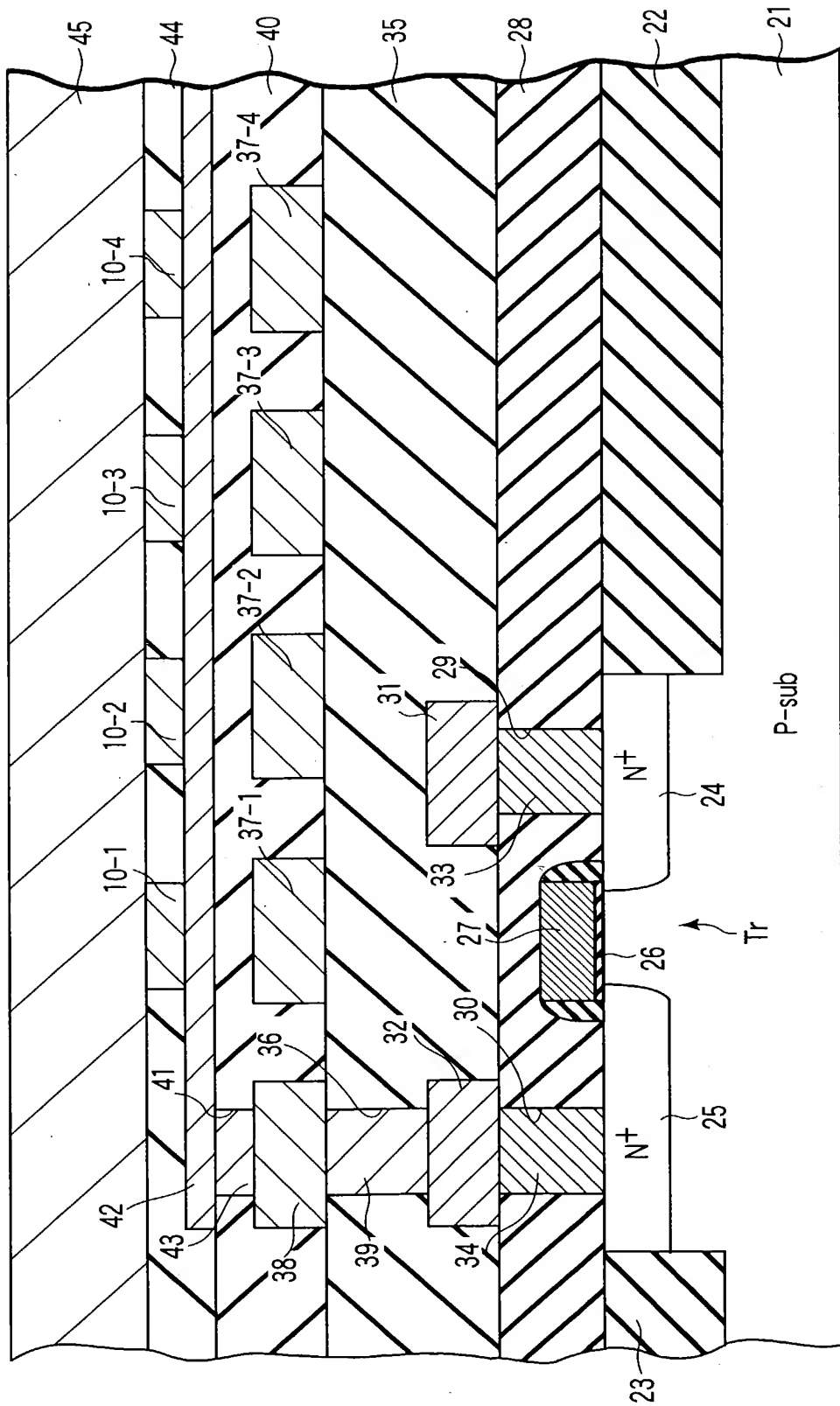


FIG. 13A

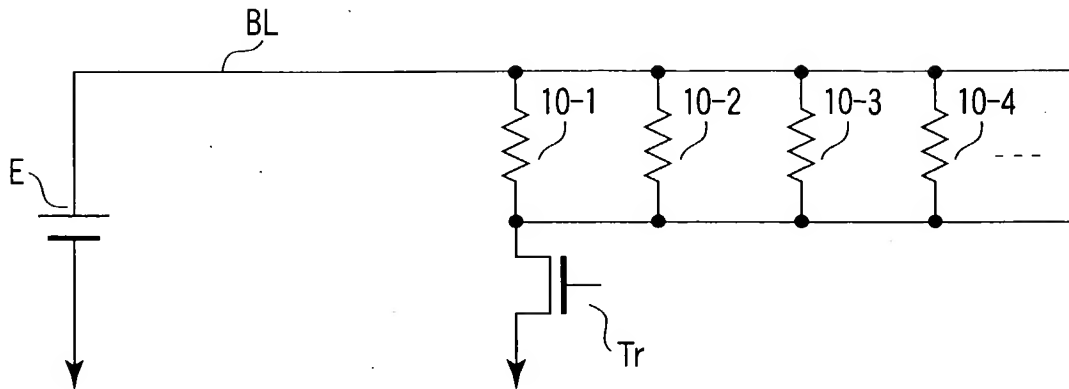


FIG. 13B

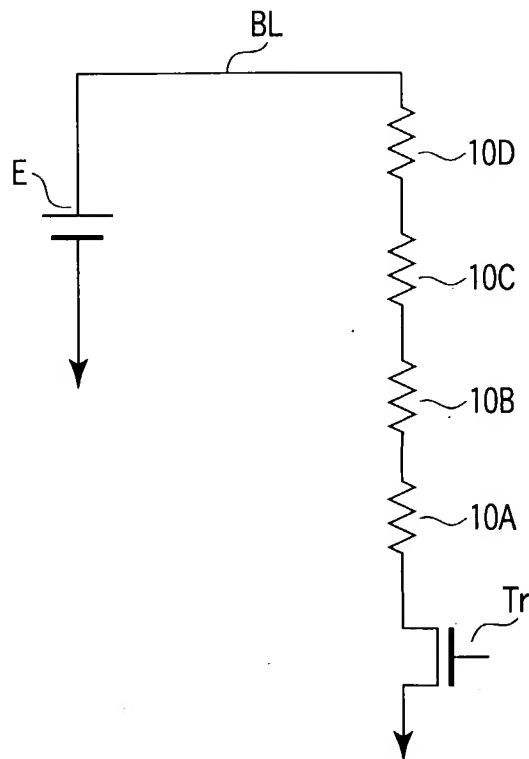


FIG. 14B



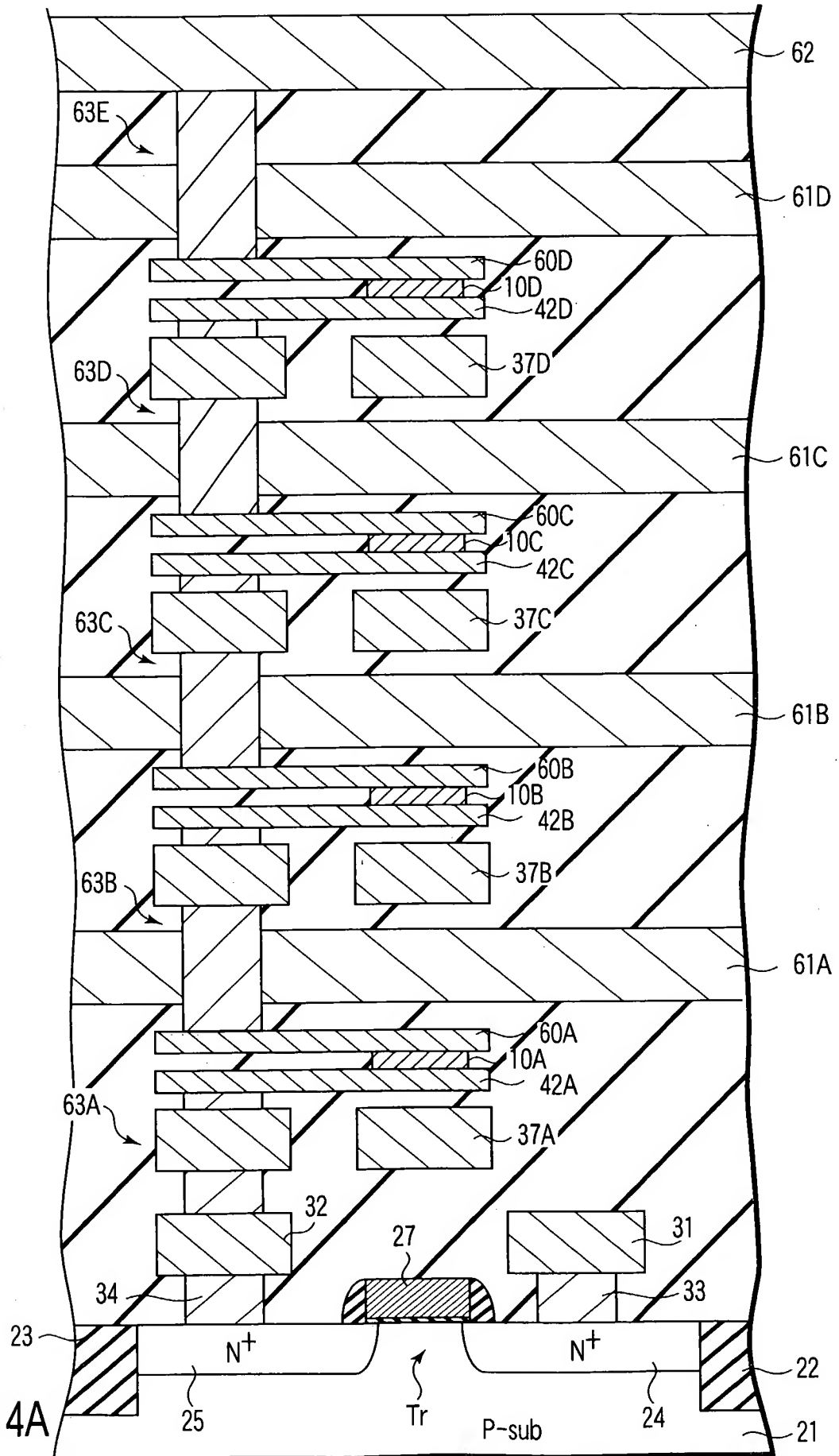


FIG. 14A

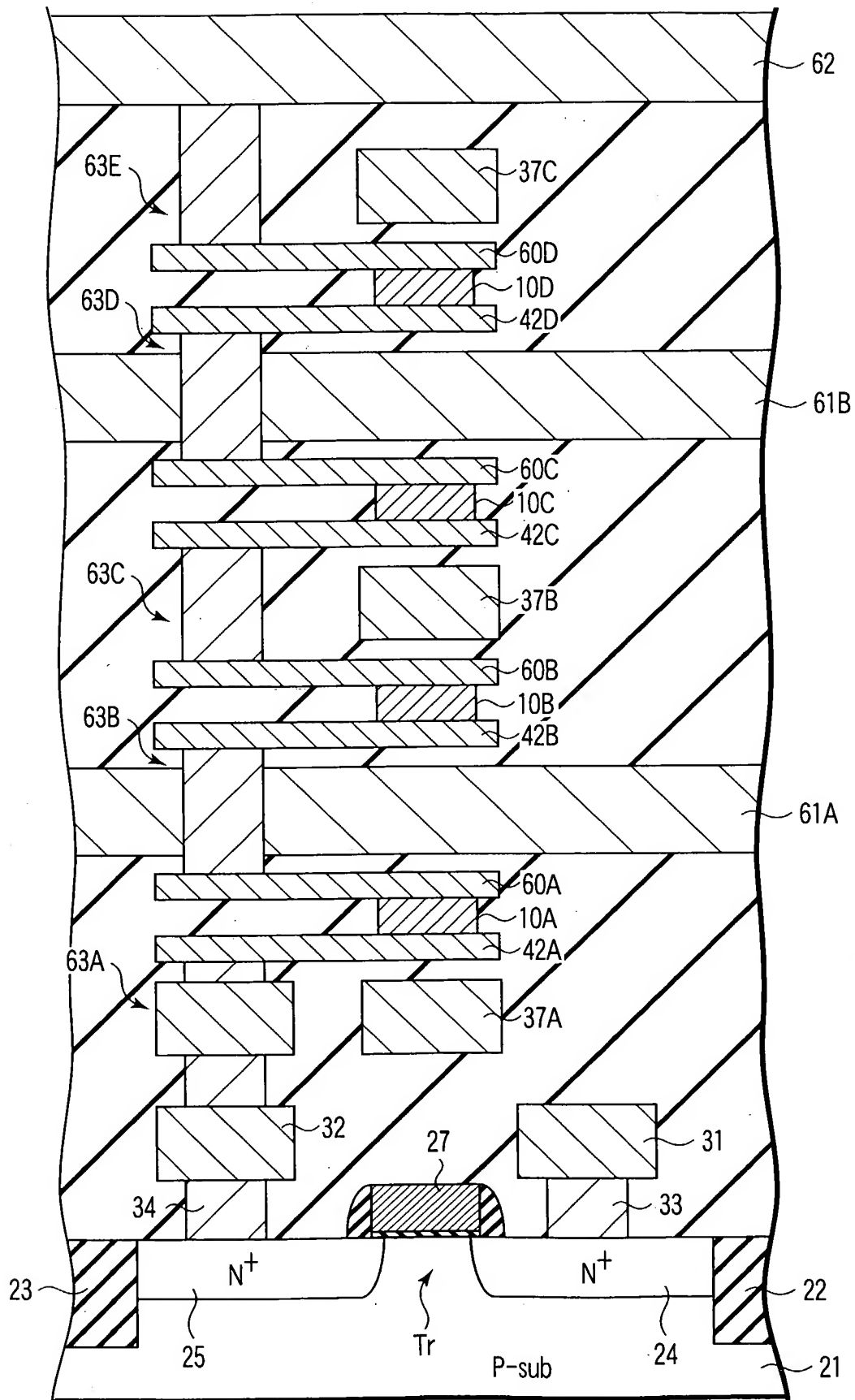
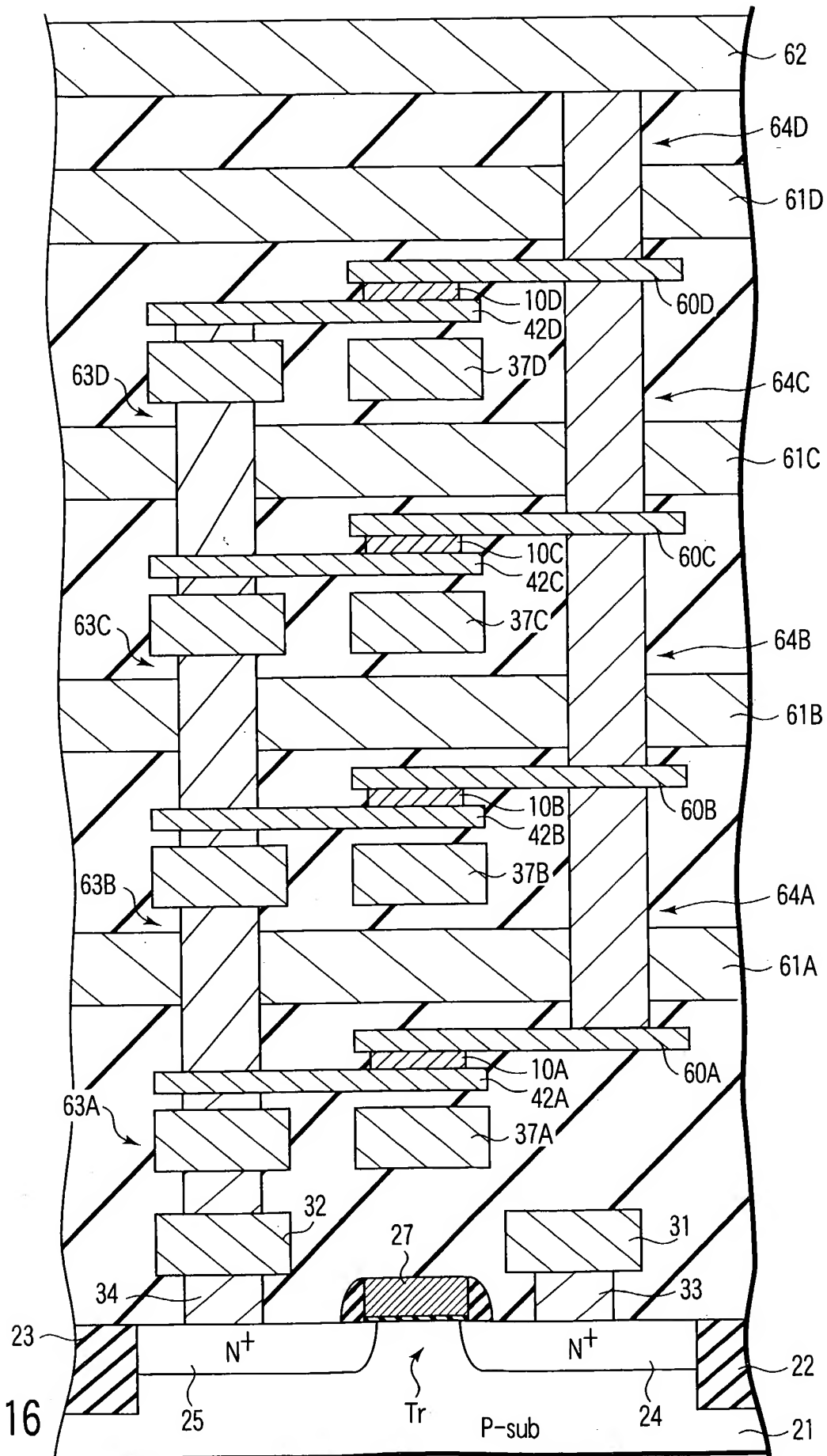


FIG. 15



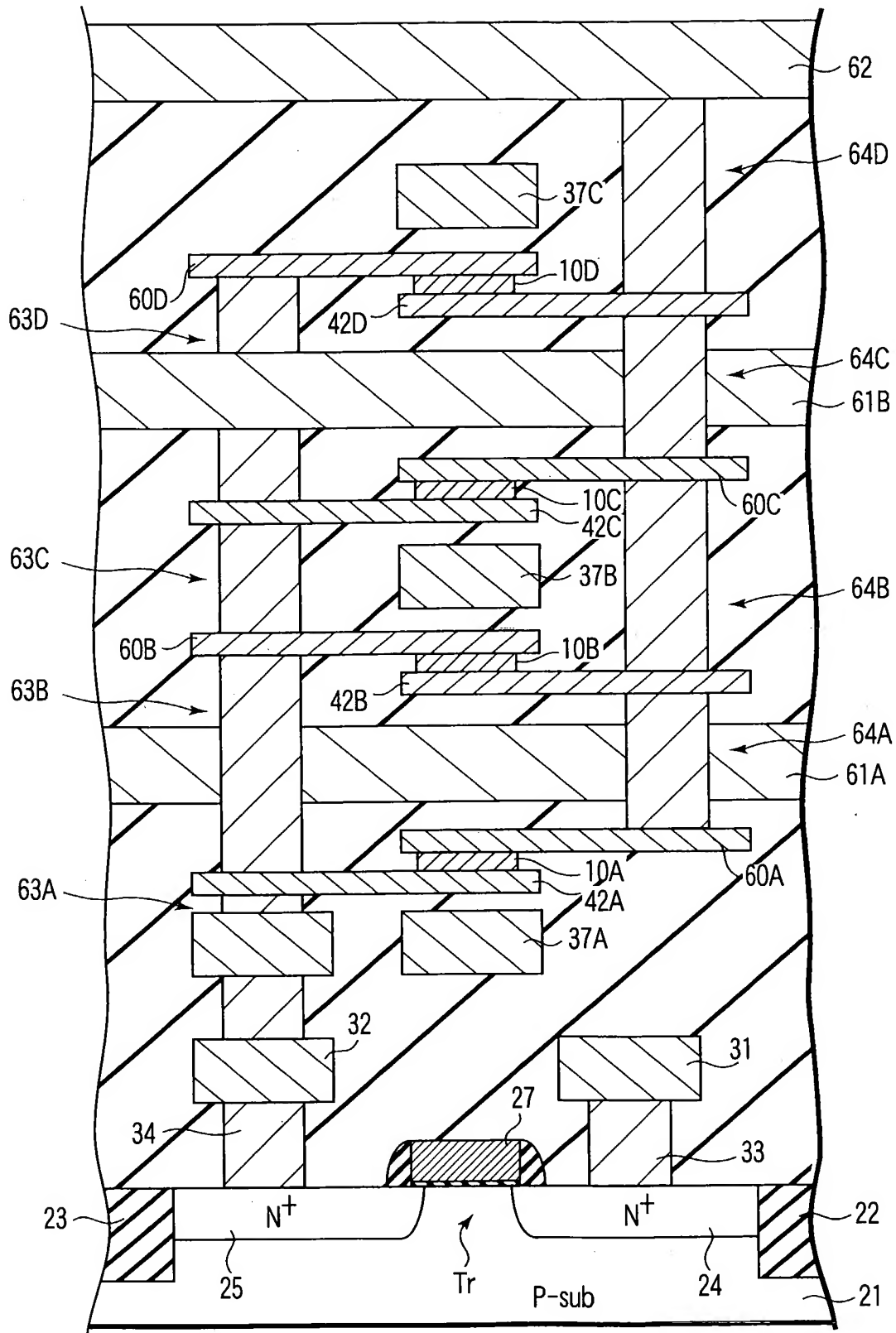


FIG. 17

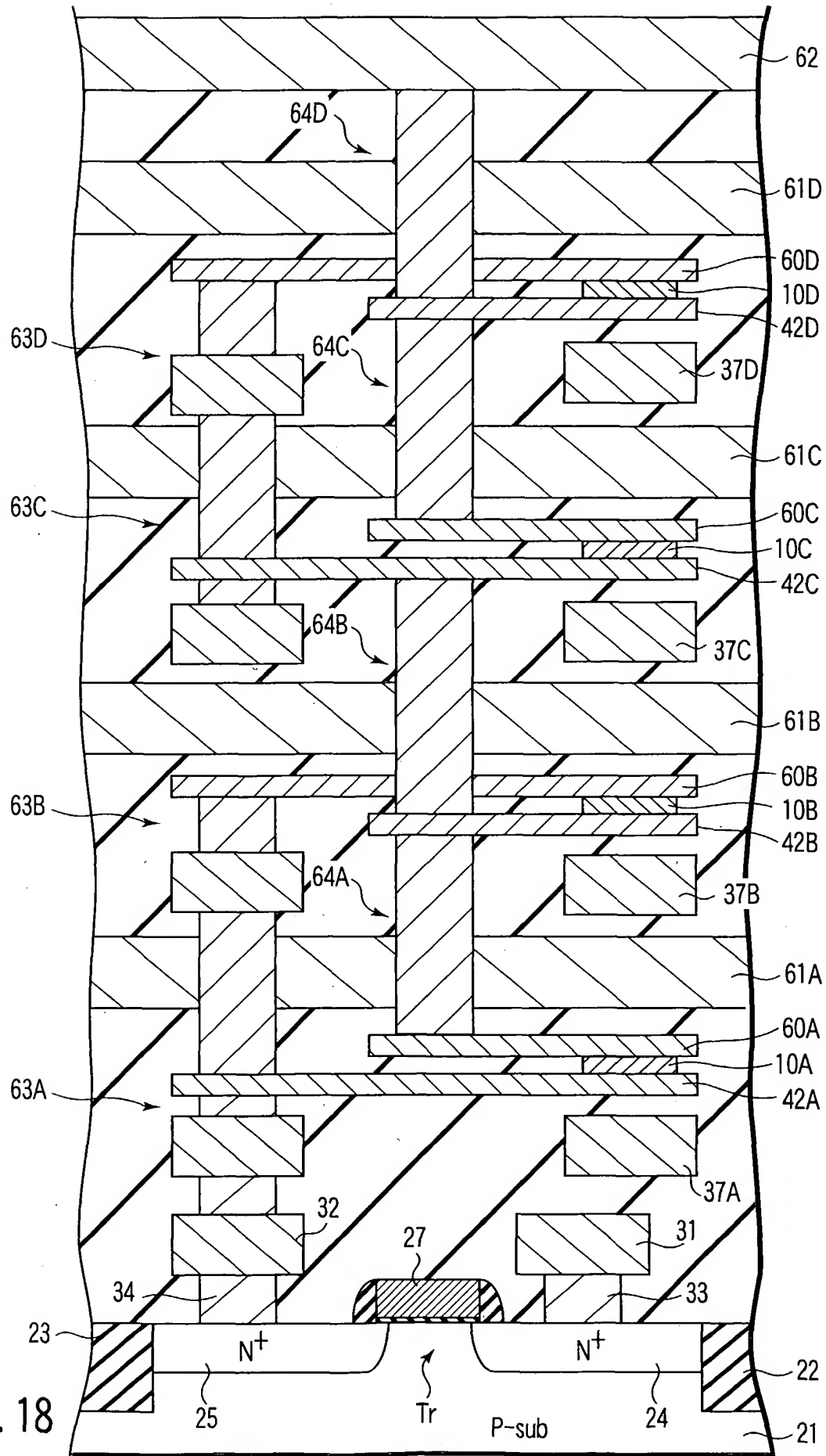


FIG. 18

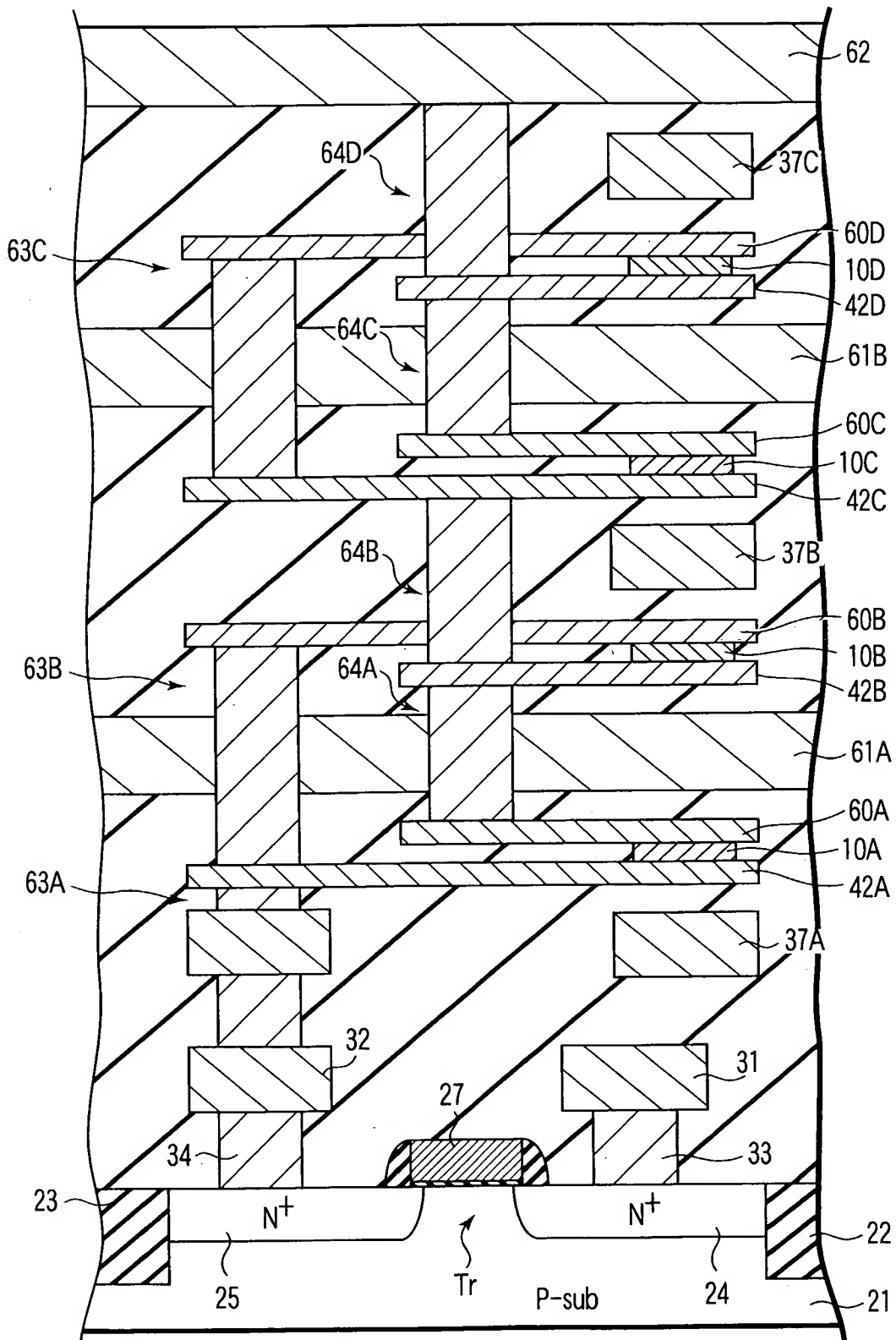


FIG. 19

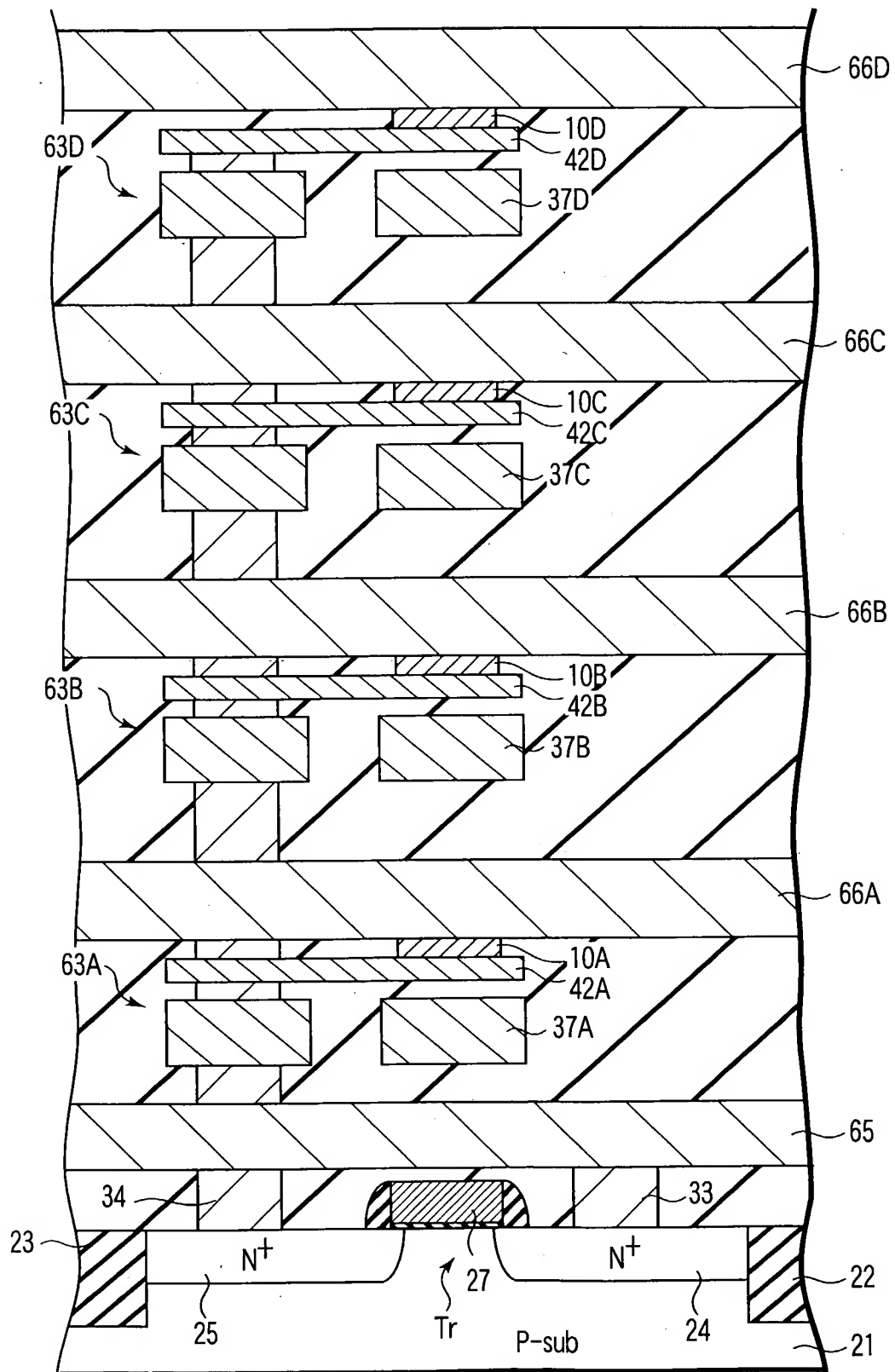


FIG. 20



FIG. 21



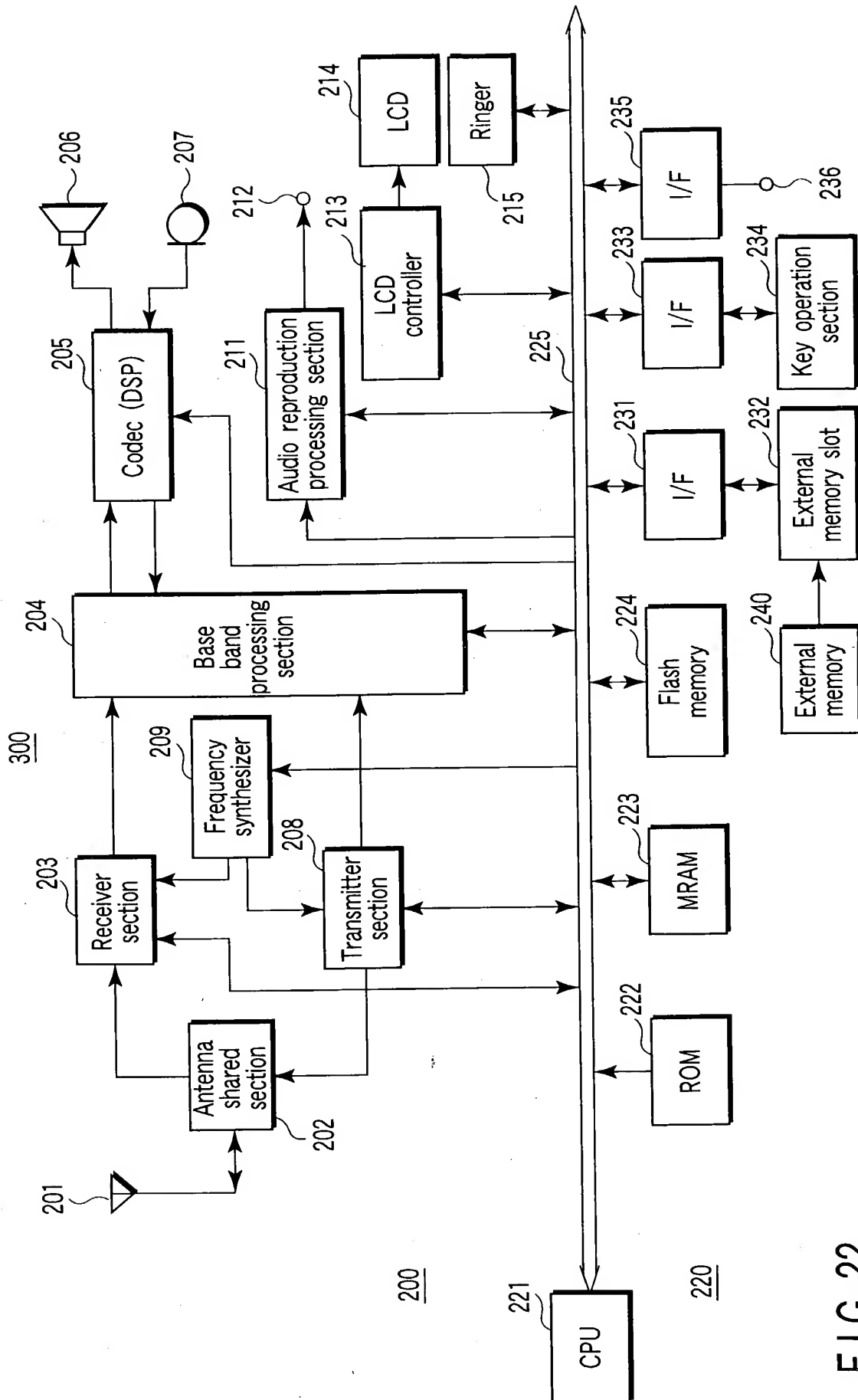


FIG. 22

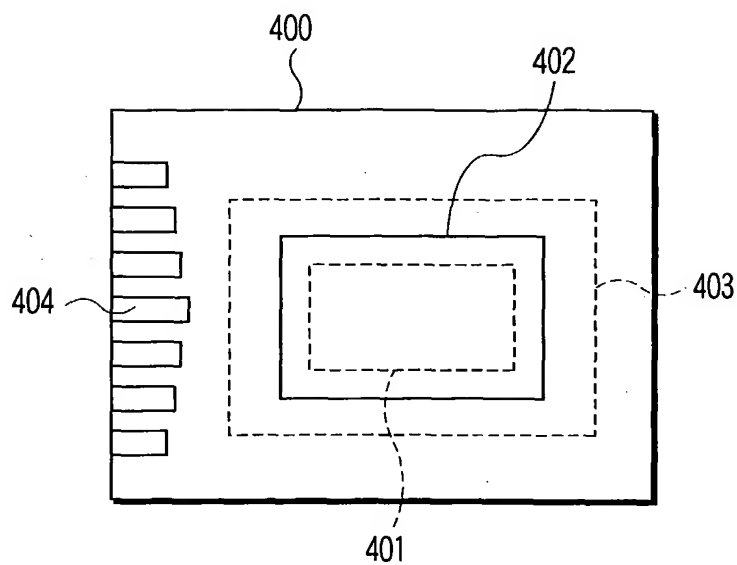
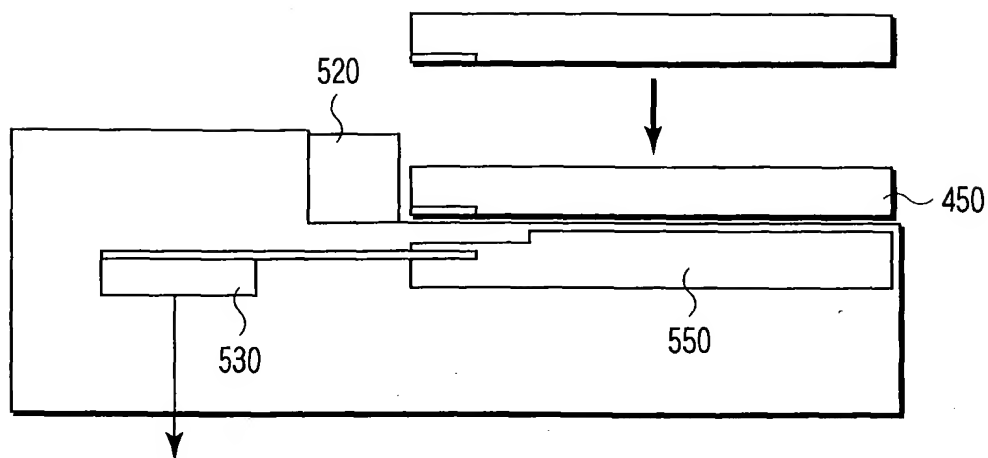


FIG. 23



Transfer first MRAM data to  
write control section

FIG. 26

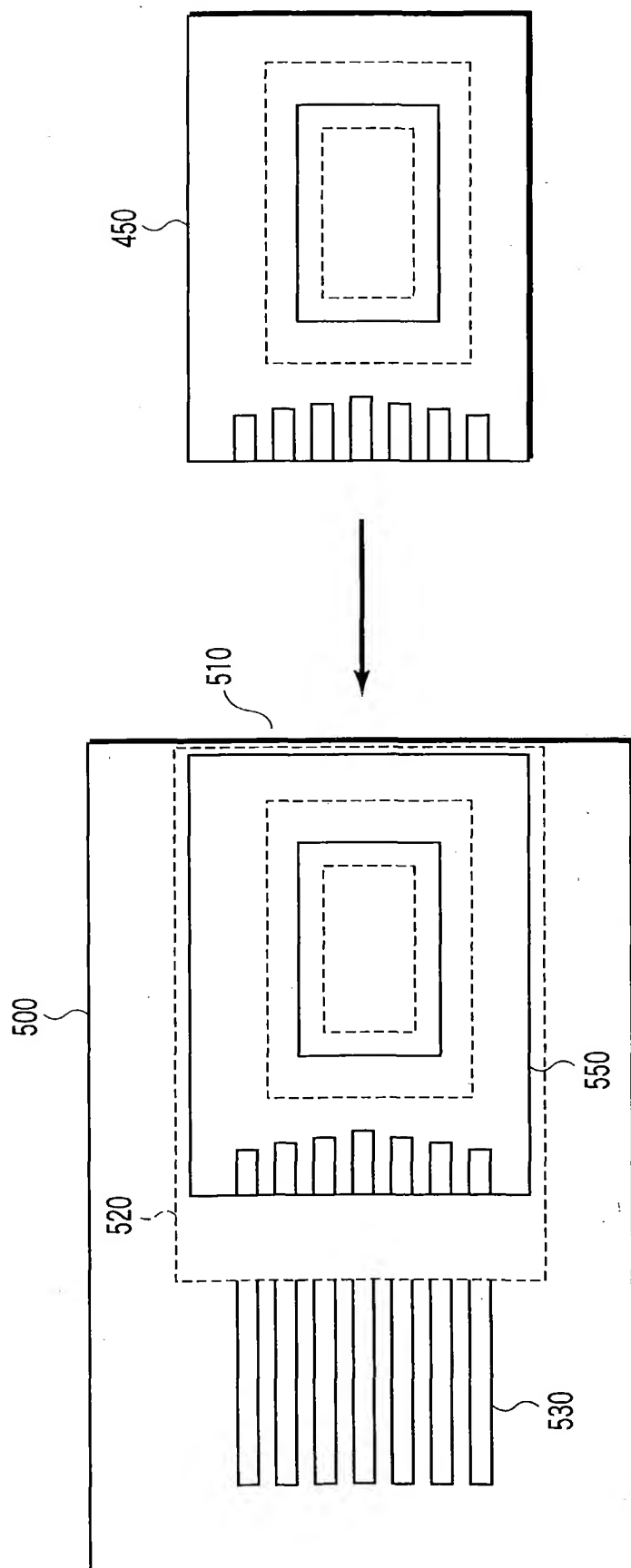


FIG. 24

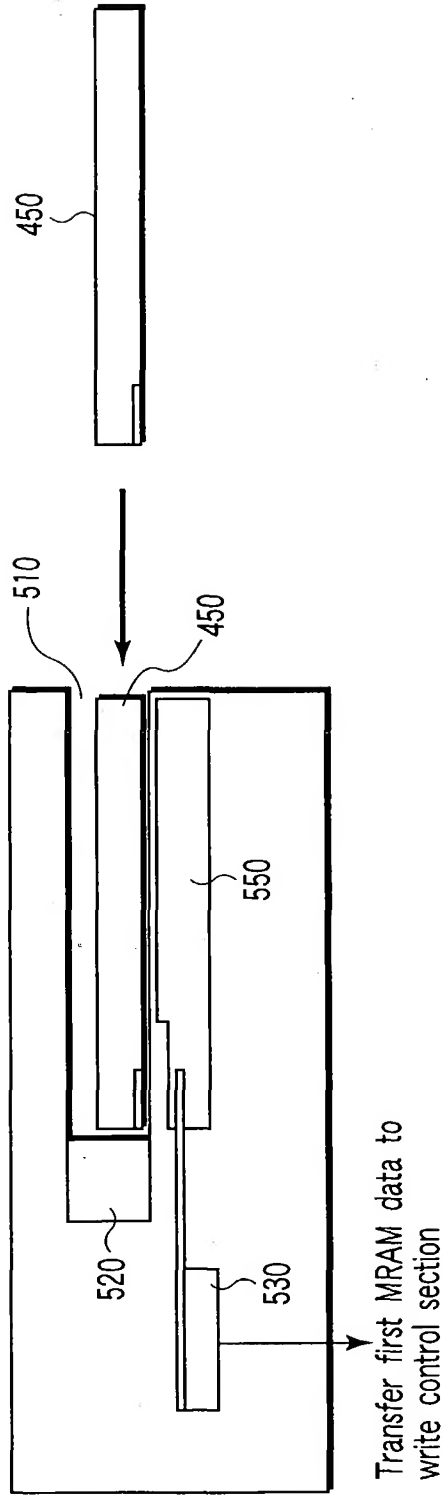


FIG. 25

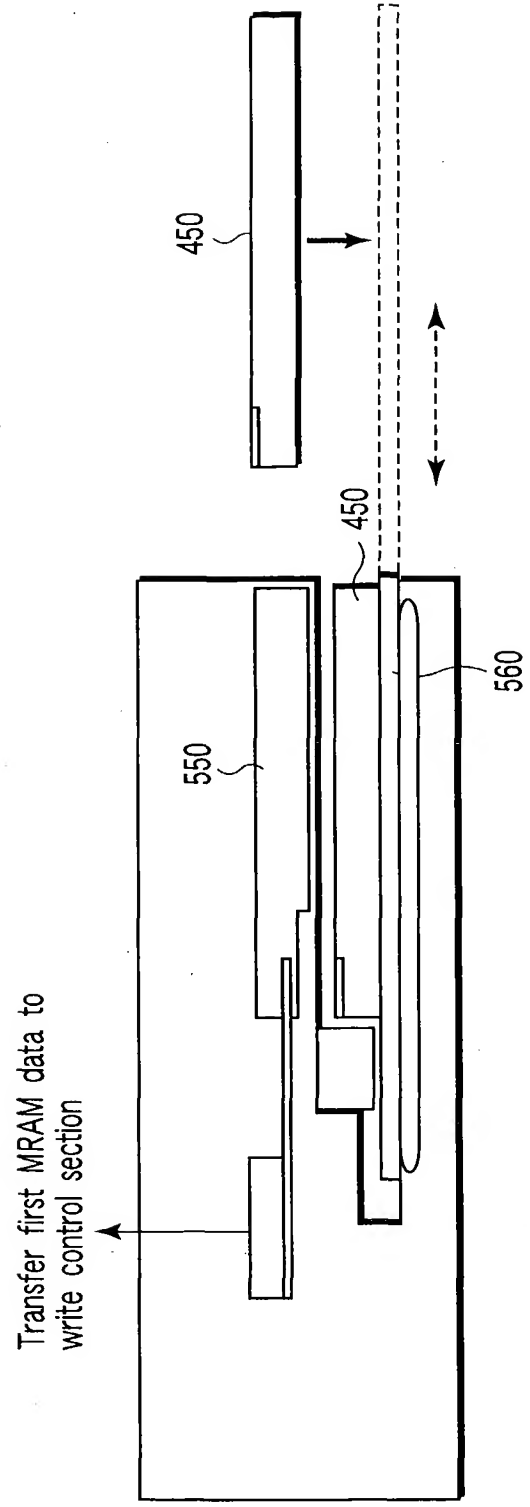


FIG. 27